UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,590	09/27/2001	Mitsuru Komiyama	F00ED0023	9688

26071 7590 05/21/2003

JUNICHI MIMURA
OKI AMERICA INC.
1101 14TH STREET, N.W.
SUITE 555
WASHINGTON, DC 20005

EXAMINER
GRAYBILL, DAVID E

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,590	KOMIYAMA ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 11 and 12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The non-described subject matter is the claim 11 limitation, wherein the first metal bump is not physically connected to the first bond of the third bonding wire, and the claim 12 limitation, wherein the metal bump is not physically connected to the first bond of the second bonding wire. To further clarify, the first metal bump and the metal bump are described as being physically connected to the first bonds at least via the conductive relay pad.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 11 and 12 the limitations that the bumps are electrically but not physically connected to the bonds via the conductive relay pad appear to be incorrect because it appears that electrical connection requires physical connection.

In the rejections infra, reference labels are generally recited only for the first recitation of identical elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 13, 14, 19-22, 25 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Takiar (5422435), or in the alternative, under 35 U.S.C. 103(a) as obvious over Takiar (5422435) in combination with O'Conner (6476506).

At column 4, line 42 to column 8, line 51, Takiar teaches the following:

13. A multi-chip package type semiconductor device, comprising: a first semiconductor chip 22 having a first terminal pad 32 and a conductive relay pad 58, the conductive relay pad including a first area and a second area, a second semiconductor chip 24, which is placed on the first semiconductor chip, the second semiconductor chip having a

second terminal pad 54, connected to the conductive relay pad in the second area; a first internal terminal 46 connected to the first terminal pad; and a second internal terminal 44 connected to the conductive relay pad in the first area.

14. A multi-chip package type semiconductor device, as in 13, further comprising an insulating substrate "carrier member", wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

19. A multi-chip package type semiconductor device, as in 13, wherein the first area and the second area are located along a side of the first semiconductor chip.

20. A multi-chip package type semiconductor device, comprising: a first semiconductor chip having a first conductive portion 32 and a second conductive portion 58, the second conductive portion having a first area and a second area; a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a third conductive portion, connected to the second conductive portion in the first area; a first internal terminal connected to the first conductive portion; and a second internal terminal connected to the second conductive portion in the second area.

21. A multi-chip package type semiconductor device, as in 20, wherein the first area and the second area are located along a side of the first semiconductor chip.

22. A multi-chip package type semiconductor device, as in 20, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

25. A multi-chip package type semiconductor device, comprising: an insulating substrate; a first conductive pattern formed on the insulating substrate; a first semiconductor chip mounted on the insulating substrate; a second conductive pattern 58 formed on the first semiconductor chip, the second conductive pattern having a first area and a second area; a second semiconductor chip mounted on the first semiconductor chip; a third conductive pattern 54 formed on the second semiconductor chip; a first wire 56 connected between the first area of the second conductive pattern and the third conductive pattern; and a second wire 60 connected between the second area of the second conductive pattern and the first conductive pattern.

26. A multi-chip package type semiconductor device, as in 25, wherein the first area and the second area are located along the side of the first semiconductor chip.

To further clarify the teaching of the conductive relay pad including a first area and a second area, the second terminal pad connected to the conductive relay pad in the second area, the second internal terminal connected to the conductive relay pad in the first area, a first wire connected between the first area of the second conductive pattern and the third conductive pattern, and a second wire connected between the second area of the second conductive pattern and the first conductive pattern, it is noted that, as cited, Takiar teaches a first and second wire connected to the conductive relay pad. Moreover, it is inherent that the first and second wire are connected [both electrically and physically] at first and second areas of the conductive relay pad. In order to further afford applicant the benefit of compact prosecution, it is noted that the scope of the claims encompasses an embodiment wherein the first and the second areas are the same area.

Although, as recited supra, the limitations of the conductive relay pad including a first area and a second area, the second terminal pad connected to the conductive relay pad in the second area, the second internal terminal connected to the conductive relay pad in the first area, a first wire connected between the first area of the second conductive pattern and the third conductive pattern, and a second wire connected between

the second area of the second conductive pattern and the first conductive pattern are inherent in the product of Takiar, Takiar does not appear to literally teach these limitations.

Nevertheless, at column 5, line 44 to column 6, line 36, O'Conner teaches a conductive relay pad 112 including a first area and a second area and a first and second wire 144, 146 connected to the first and second area, respectively. In addition, it would have been obvious to combine the product of O'Conner with the product of Takiar because it would provide high density bond pads.

Claims 23, 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Takiar and O'Conner as applied to claims 20 and 25.

As cited, Takiar teaches the following:

24. A multi-chip package type semiconductor device, as in 20, further comprising: a first wire 60, the first wire having one end connected to the second terminal and the other end connected to the second conductive portion.

27. A multi-chip package type semiconductor device, as in 25, further comprising: wherein the first wire is connected to the first area and the second wire is connected to the third conductive pattern.

However, Takiar does not appear to explicitly teach the wires connected through bumps or the following:

23. A multi-chip package type semiconductor device, as in 20, wherein the first area and the second area are spaced from each other.

28. A multi-chip package type semiconductor device, as in 25, wherein the first area and the second area are spaced each other.

Nonetheless, as cited supra, O'Conner teaches these limitations. Furthermore, it would have been obvious to combine the product of O'Conner with the product of Takiar because it facilitate wire connection and provide high density bond pads.

Claims 1, 2, 15 and 16 are rejected under 35 U.S.C. 103(a) as obvious over Takiar (5422435), or the combination of Takiar (5422435) and Haba (6376904), or the combination of Takiar (5422435) and O'Conner (6476506), or the combination of Takiar (5422435), Haba (6376904) and O'Conner (6476506).

As cited supra, Takiar teaches the following:

1. A multi-chip package type semiconductor device, comprising: an insulating substrate having thereon a first conductive pattern 46 and a second conductive pattern 44; a first semiconductor chip having a first internal circuit on the insulating substrate, the first semiconductor chip having a

first terminal pad connecting to the first internal circuit and a conductive relay pad isolated from the first terminal pad, and the conductive relay pad including a first area and a second area; a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit; a first bonding wire [not labeled] connecting the first terminal pad to the first conductive pattern; a second bonding wire 60 connecting the second conductive pattern to the conductive relay pad in the first area; and a third bonding wire 56 connecting the conductive relay pad in the second area to the second terminal pad.

2. A multi-chip package type semiconductor device, as in 1, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

15. A multi-chip package type semiconductor device, comprising: an insulating substrate having a first and second conductive patterns thereon; a first semiconductor chip on the insulating substrate, the first semiconductor chip having a first internal circuit, a first terminal pad connecting to the first internal circuit and a conductive relay pad isolated from the first terminal pad; a second semiconductor chip on the first

semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit, a first bonding wire connecting the first terminal pad to the first conductive pattern; a second bonding wire connecting the second conductive pattern to the conductive relay pad; and a third bonding wire connecting the conductive relay pad to the second terminal pad.

16. A multi-chip package type semiconductor device, as in 15, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

To further clarify the teaching of a second bonding wire connecting the second conductive pattern to the conductive relay pad in the first area; and a third bonding wire connecting the conductive relay pad in the second area to the second terminal pad, it is noted that, as cited, Takiar teaches a second and third wire connected to the conductive rely pad. Moreover, it is inherent that the second and third wire are connected [both electrically and physically] at first and second areas of the conductive relay pad. In order to further afford applicant the benefit of compact prosecution, it is noted that the scope of the claims encompasses an embodiment wherein the first and the second areas are the same area.

Although, as recited supra, the limitations of a second bonding wire connecting the second conductive pattern to the conductive relay pad in the first area; and a third bonding wire connecting the conductive relay pad in the second area to the second terminal pad are inherent in the product of Takiar, Takiar does not appear to literally teach these limitations.

Nevertheless, as cited supra, O'Conner teaches a conductive relay pad 112 including a first area and a second area and a first and second wire 144, 146 connected to the first and second area, respectively. Therefore, it would have been obvious to combine the product of O'Conner with the product of the applied prior art because it would provide high density bond pads.

However, Takiar does not appear to explicitly teach wherein the lengths of the first, second and third bonding wire are approximately the same

Nevertheless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular relative lengths because, as cited, Takiar teaches that wire bond length is a result effective variable, and applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie

that the product would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In any case, at column 6, lines 6-12, Haba teaches wherein the lengths of first, second and third bonding wires 440a, 440b, 440c, respectively, are approximately the same. In addition, it would have been obvious to combine the product of Haba with the product of Takiar, because it would provide desirable electrical properties.

Claims 3-12, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Takiar (5422435) and O'Conner (6476506), or the combination of Takiar (5422435), Haba (6376904) and O'Conner (6476506) as applied to claims 2 and 16.

As previously cited, Takiar teaches the following:

3. A multi-chip package type semiconductor device, as in 2, further comprising wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the second conductive pattern and the second bond as the ending connection of the second bonding wire is made at the first area, and wherein the first bond as the beginning connection of the third bonding wire is preformed at the conductive relay pad in the second area and the second bond as the ending connection of the third bonding wire is made at the second terminal pad.

4. A multi-chip package type semiconductor device, as in 2, further comprising, wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the conductive relay pad in the first area and the second bond as the ending connection of the second bonding wire is made at the second conductive pattern, and wherein the first bond as the beginning connection of the

third bonding wire is preformed at the second terminal pad and the second bond as the ending connection of the third bonding wire is made at the second area.

5. A multi-chip package type semiconductor device, as in 3, wherein the conductive relay pad is rectangularly-shaped [square], and is formed on the periphery of the first semiconductor chip, and a longer side [the top side in the length direction] of the rectangularly-shaped conductive relay pad is parallel to a side [the top side] of the first semiconductor chip.

6. A multi-chip package type semiconductor device, as in 3, wherein the conductive relay pad is rectangularly-shaped, and is formed on the periphery of the first semiconductor chip, and a shorter side [the top side in the width direction] of the rectangularly-shaped conductive relay pad is parallel to a side [the top side] of the first semiconductor chip.

8. A multi-chip package type semiconductor device, as in 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on the periphery of the first semiconductor chip, and a longer side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

9. A multi-chip package type semiconductor device, as in 4, wherein the conductive relay pad is rectangularly-shaped, and is

formed on the periphery of the first semiconductor chip, and a shorter side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

11. A multi-chip package type semiconductor device, as in 3, wherein the first area is not physically connected to the first bond of the third bonding wire, but is electrically connected to the first bond of the third bonding wire via the conductive relay pad.

12. A multi-chip package type semiconductor device, as in 4, wherein the second area is not physically connected to the first bond of the second bonding wire, but is electrically connected to the first bond of the second bonding wire via the conductive relay pad.

17. A multi-chip package type semiconductor device, as in 16, further comprising, wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the second conductive pattern and the second bond as the ending connection of the second bonding wire is made at conductive relay pad, and wherein the first bond as the beginning connection of the third bonding wire is

preformed at the conductive relay pad and the second bond as the ending connection of the third bonding wire is made at the second terminal pad.

18. A multi-chip package type semiconductor device, as in 16, further comprising, wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the conductive pattern and the second bond as the ending connection of the second bonding wire is made at the conductive relay pad, and wherein the first bond as the beginning connection of the third bonding wire is preformed at the second terminal pad and the second bond as the ending connection of the third bonding wire is made at the conductive relay pad.

However, Takiar does not appear to explicitly teach the wires connected through bumps or the following:

7. A multi-chip package type semiconductor device, as in 6, wherein the first area of the rectangularly-shaped conductive relay pad is closer to a side of the first semiconductor chip than the second area.

10. A multi-chip package type semiconductor device, as in 9, wherein the first area of the rectangularly-shaped conductive relay pad is closer to a side of the first semiconductor chip than the second area.

Still, as cited supra, O'Conner teaches these limitations. Furthermore, it would have been obvious to combine the product of O'Conner with the product of Takiar because it would facilitate wire connection and provide high density bond pads.

Claims 5, 6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Takiar (5422435) and O'Conner (6476506), or the combination of Takiar (5422435), Haba (6376904) and O'Conner (6476506) as applied to claims 3 and 4, and further in combination with Hill (6091825).

As previously cited, Takiar teaches the following:

5. A multi-chip package type semiconductor device, as in 3, wherein the conductive relay pad is rectangularly-shaped [square], and is formed on the periphery of the first semiconductor chip, and a side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

6. A multi-chip package type semiconductor device, as in 3, wherein the conductive relay pad is rectangularly-shaped, and is formed on the periphery of the first semiconductor chip, and a

side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

8. A multi-chip package type semiconductor device, as in 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on the periphery of the first semiconductor chip, and a side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

9. A multi-chip package type semiconductor device, as in 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on the periphery of the first semiconductor chip, and a side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

However, Takiar does not appear to appear to literally teach a longer and a shorter side of a rectangularly-shaped conductive bond pad, each side parallel to a side of a first semiconductor chip.

Notwithstanding, at column 3, line 38 to column 4, line 10, Hill literally teaches a longer and a shorter side of a rectangularly-shaped conductive bond pad 154a, each side parallel to a side of a first semiconductor chip 150. Moreover, it would have been obvious to combine the product of Hill with the product of Takiar because it would provide high density bond pads.

Applicant's amendment and remarks filed 2-11-3 have been fully considered, are addressed in the rejection supra, and are further addressed infra.

Applicant alleges that Takiar does not disclose a first bonding wire connecting the first terminal pad to the first conductive pattern.

This allegation is respectfully traversed because, at column 6, lines 15-18, Takiar explicitly teaches a first bonding wire [not labeled] connecting the first terminal pad 32 to the first conductive pattern 46.

Also, applicant contends that Haba does not teach the limitations, "a first bonding wire connecting the first terminal pad to the first conductive pattern," or "the lengths of the first, second and third bonding wire are approximately the same."

This contention is respectfully deemed unpersuasive because Haba is not relied on in the rejection for these teachings. In particular, Haba is relied on only for a general teaching of analogous prior art wherein the lengths of first, second and third bonding wires are approximately the same, and is not necessarily relied on for the teachings for which Takiar is relied on.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-308-1782306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
19-May-03